Electronic Ack	Electronic Acknowledgement Receipt				
EFS ID:	2275901				
Application Number:	10072145				
International Application Number:					
Confirmation Number:	1448				
Title of Invention:	Semiconductor device and method of providing regions of low substrate capacitance				
First Named Inventor/Applicant Name:	Guy E. Averett				
Correspondence Address:	ON Semiconductor Patent Administration Dept - MD A700 P.O. Box 62890 - Phoenix AZ 85082-2890 US 6022443169				
Filer:	Kevin Brian Jackson				
Filer Authorized By:					
Attorney Docket Number:	ONS00317				
Receipt Date:	03-OCT-2007				
Filing Date:	07-FEB-2002				
Time Stamp:	17:13:43				
Application Type:	Utility under 35 USC 111(a)				
Payment information:					
Submitted with Payment	no				

File Listing:

Number	Document Description	File Name	/Message Digest	Part /.zip	(if appl.)
1	Amendment - After Non-Final Rejection	ONS00317Amendment_100 32007.pdf	439084	no	12
			6b2bt304a70eat916f558a5fb4197d6c4 72cf88l		
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New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.